

EXAMINER'S AMENDMENT

This action is in response to Applicant's filings on June 15, 2009.

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.
2. The Examiner tried to contact Mr. Mark Weichselbaum on October 8, 2009, but no reply was received. In an effort to expedite prosecution, the Examiner has performed the following amendment in an effort to correct what are believed to be typos in the Specification.

The application has been amended as follows:

SPECIFICATION: On Page 7 Line 19, replace "12V battery" with "--14V battery--.

On Page 10 Line 9, replace "14V" with "--60V--.

On Page 10 Line 17, replace " $P(T1) + V_{ds} * I(R2)$ " with

$--P(T1) = V_{ds} * I(R2)--.$

3. The following is an examiner's statement of reasons for allowance:
4. Claims 7-9 and 11-13 recite a device for protecting an electronic module disposed in a control device in a multi-voltage on-board electrical system having an accumulator with a low on-board electrical system voltage against short circuiting to a high on-board electrical system voltage that includes among other components: a MOSFET transistor having a drain source path inserted between a control device connection and a connection of the electronic module with a source connected to the connection of the electronic module, a drain connected to the control

device connection, and gate connected to a positive pole of the first accumulator via a gate resistor; wherein when a short circuit to the high on board electrical system voltage is conducted to said drain, said MOSFET transistor turns on or remains turned on; wherein said MOSFET transistor has a threshold voltage and, in an event of a short circuit to a highest voltage on the on-board electrical system active at the device connection, a source voltage of said transistor is limited to a value $V_s = V_{bat1} - V_{th}$, where V_s is the source voltage, V_{bat1} is the low on-board voltage, and V_{th} is the threshold voltage of said transistor. The featured limitations discussed above in combination with the other limitations of the claims is not anticipated by the prior art of record, nor would it have been obvious to one having ordinary skill in the art to modify the prior art of record in order to make the aforementioned limitations unpatentable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER J. CLARK whose telephone number is (571)270-1427. The examiner can normally be reached on M-F, 10:00-6:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Fureman can be reached on 571-272-2391. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

10/12/2009

/Ronald W Leja/
Primary Examiner, Art Unit 2836

CJC
10/9/2009